

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5193
thru
2N5195

SILICON PNP POWER TRANSISTORS

... for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192

4 AMPERE
POWER TRANSISTORS
SILICON PNP
40-80 VOLTS

***MAXIMUM RATINGS**

Rating	Symbol	2N5193	2N5194	2N5195	Unit
Collector-Emitter Voltage	V _{CEO}	40	60	80	Vdc
Collector-Base Voltage	V _{CB}	40	60	80	Vdc
Emitter-Base Voltage	V _{EB}	← 5.0 →			Vdc
Collector Current	I _C	← 4.0 →			Adc
Base Current	I _B	← 1.0 →			Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	← 40 →			Watts
		← 320 →			mW/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	← -65 to +150 →			°C/W

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ _{JC}	3.12	°C/W

***ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)**

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) (I _C = 0.1 Adc, I _B = 0)	V _{CEO(sus)}	40 60 80		Vdc
Collector Cutoff Current (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0) (V _{CE} = 80 Vdc, I _B = 0)	I _{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V _{CE} = 40 Vdc, V _{BE(off)} = 1.5 Vdc) 2N5193 (V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc) 2N5194 (V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc) 2N5195 (V _{CE} = 40 Vdc, V _{BE(off)} = 1.5 Vdc, 2N5193 T _C = 125°C) (V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc, 2N5194 T _C = 125°C) (V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc, 2N5195 T _C = 125°C)	I _{CEX}	— — — — —	0.1 0.1 0.1 2.0 2.0	mAdc
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0)	I _{CBO}	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mAdc

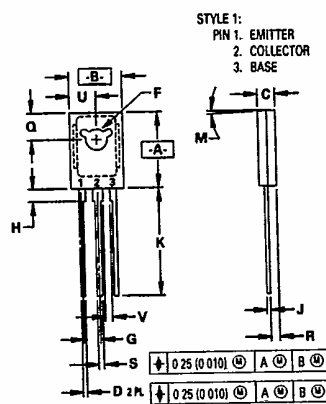
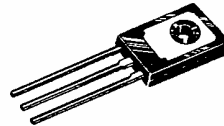
ON CHARACTERISTICS

DC Current Gain (1) (I _C = 1.5 Adc, V _{CE} = 2.0 Vdc)	h _{FE}	25 25 20	100 100 80	—
(I _C = 4.0 Adc, V _{CE} = 2.0 Vdc)		10 10 7.0	— — —	
Collector-Emitter Saturation Voltage (1) (I _C = 1.5 Adc, I _B = 0.15 Adc) (I _C = 4.0 Adc, I _B = 1.0 Adc)	V _{CE(sat)}	— —	0.6 1.4	Vdc
Base-Emitter On Voltage (1) (I _C = 1.5 Adc, V _{CE} = 2.0 Vdc)	V _{BE(on)}	—	1.2	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 10 Vdc, f = 1.0 MHz)	f _T	2.0	—	MHz
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*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.39 BSC		0.094 BSC	
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-06
TO-225AA TYPE

FIGURE 1 – DC CURRENT GAIN

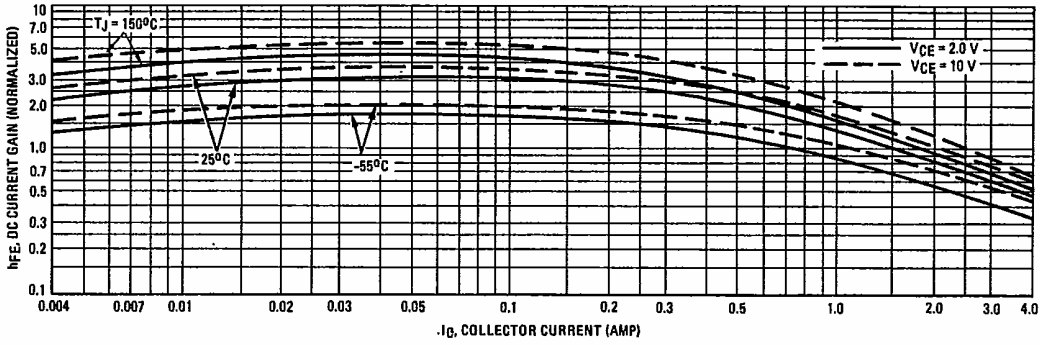


FIGURE 2 – COLLECTOR SATURATION REGION

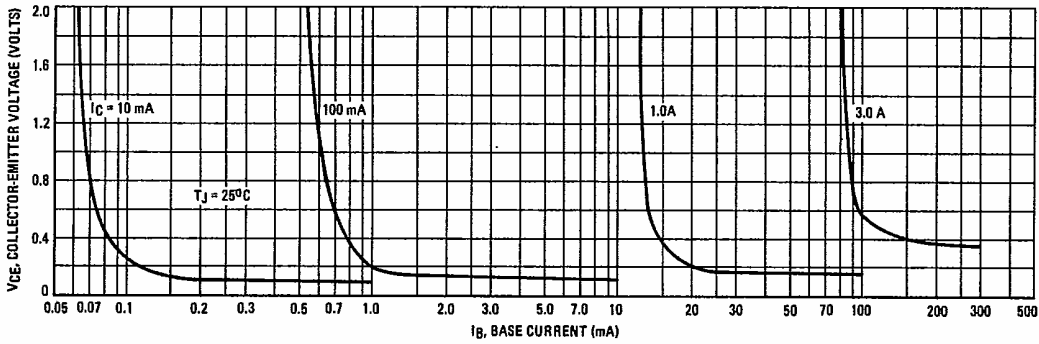


FIGURE 3 – "ON" VOLTAGE

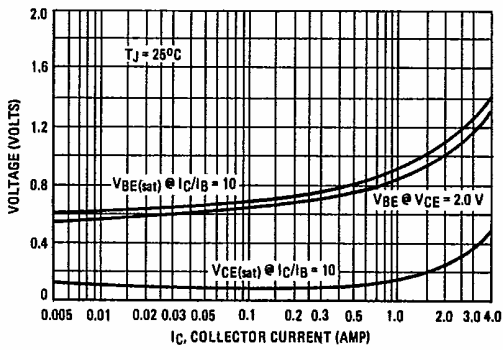


FIGURE 4 – TEMPERATURE COEFFICIENTS

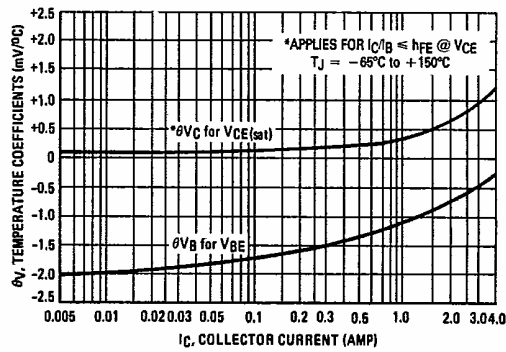


FIGURE 5 - COLLECTOR CUT-OFF REGION

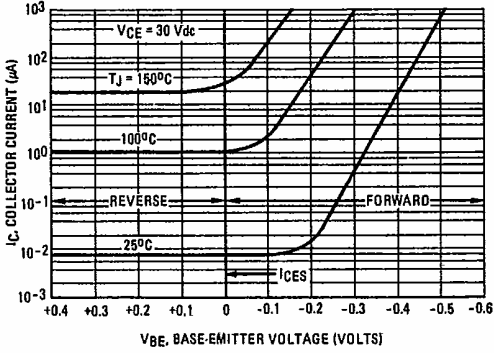


FIGURE 6 - EFFECTS OF BASE-EMITTER RESISTANCE

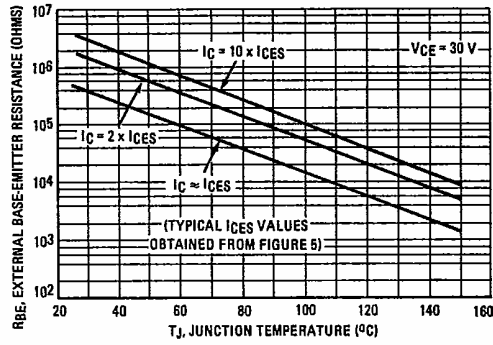


FIGURE 7 - SWITCHING TIME EQUIVALENT CIRCUIT

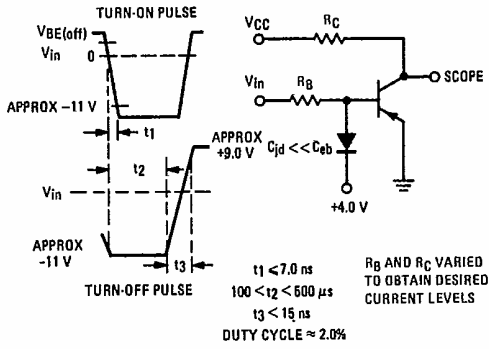


FIGURE 8 - CAPACITANCE

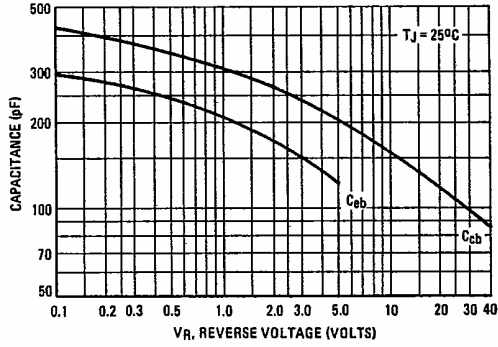


FIGURE 9 - TURN-ON TIME

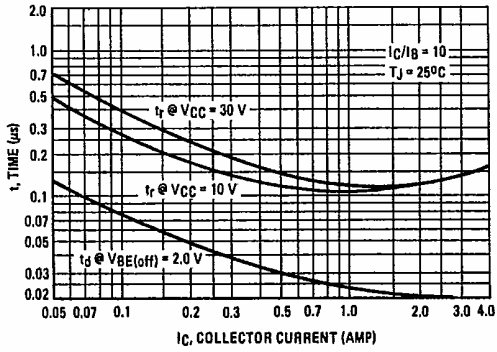


FIGURE 10 - TURN-OFF TIME

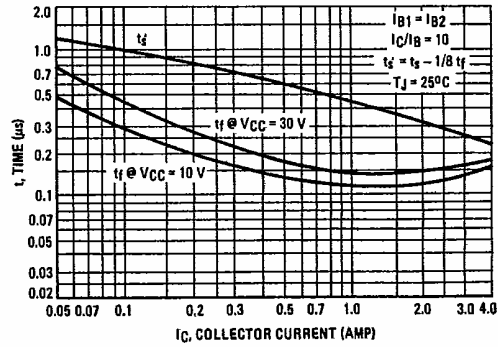
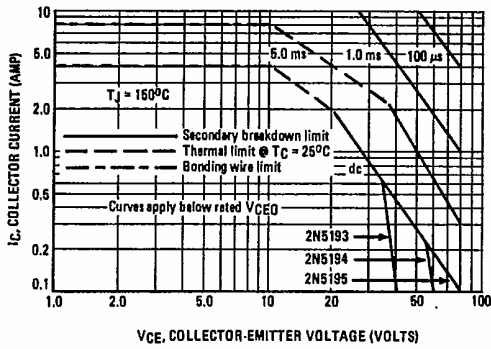


FIGURE 11
RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA

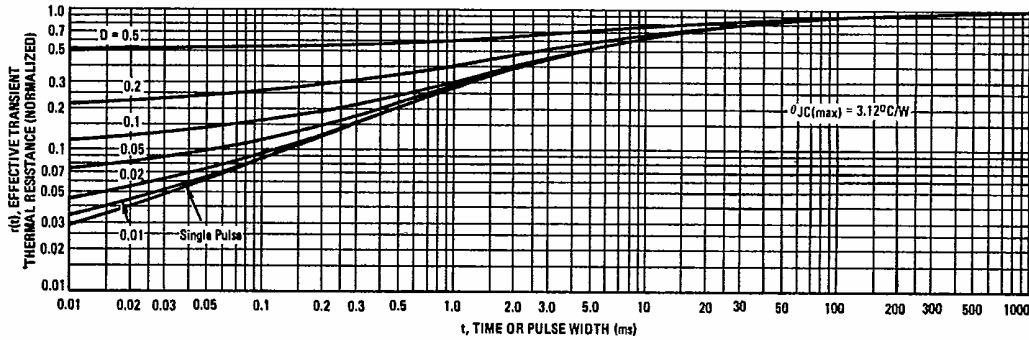


Note 1:

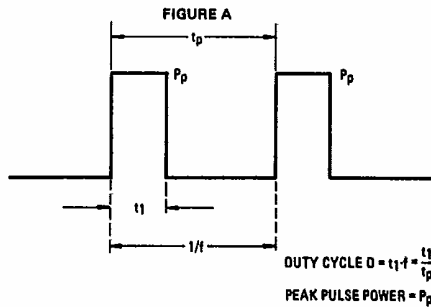
There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)} = 150^\circ\text{C}$. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 -- THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC} .

Example:

The 2N5193 is dissipating 50 watts under the following conditions: $t_1 = 0.1$ ms, $t_p = 0.5$ ms. ($D = 0.2$).

Using Figure 12, at a pulse width of 0.1 ms and $D = 0.2$, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$